Topic 8

Sequential Circuits[1]

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Rabaey Chapter 7

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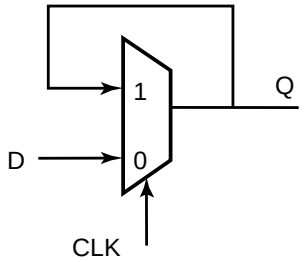
[1] Based on slides from Prentice-Hall

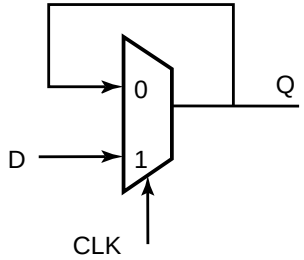
Mux-Based Latches

Negative latch (transparent when CLK= 0)



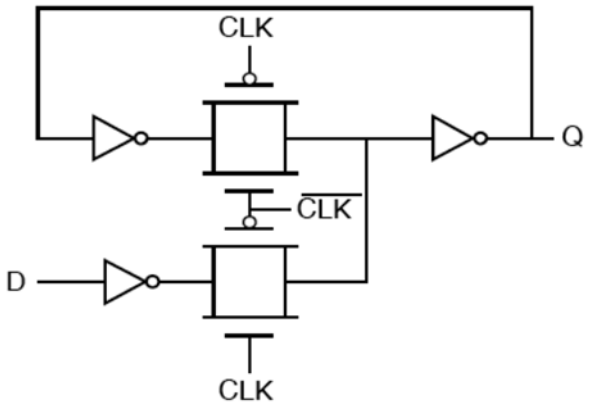
$$Q = \overline{Clk} \cdot Q + Clk \cdot In$$

Positive latch (transparent when CLK= 1)

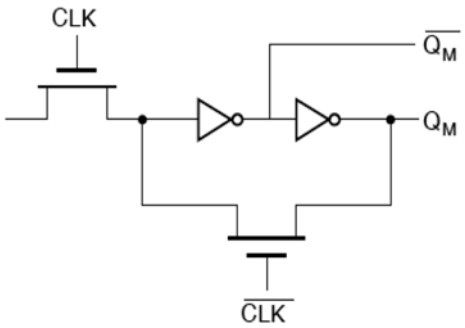


$$Q = Clk \cdot Q + \overline{Clk} \cdot In$$

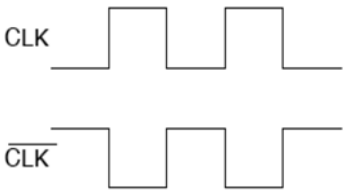
Mux-Based Latch



Mux-Based Latch

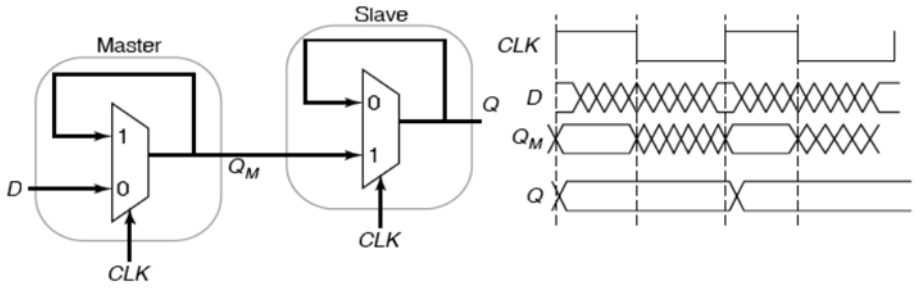


NMOS only



Non-overlapping clocks

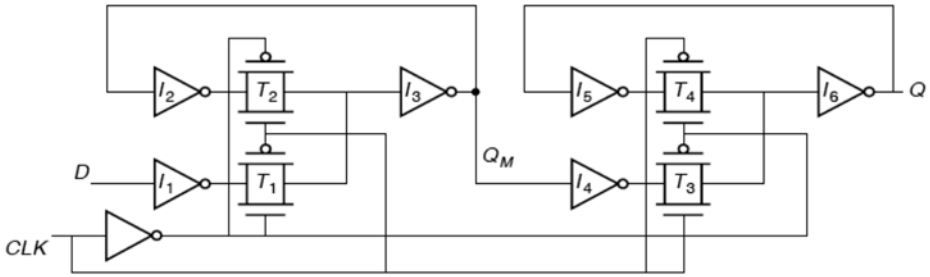
Master-Slave (Edge-Triggered) Register



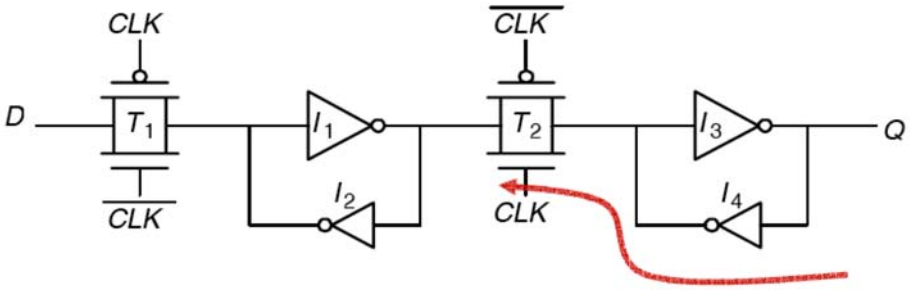
Two opposite latches trigger on edge
Also called master-slave latch pair

Master-Slave Register

Multiplexer-based latch pair

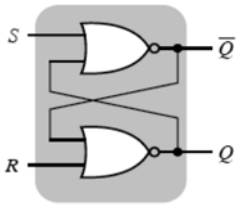


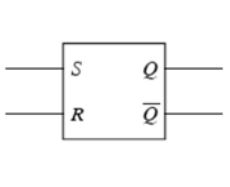
Reduced Clock Load Master-Slave Register



Overpowering the Feedback Loop – Cross-Coupled Pairs

NOR-based set-reset



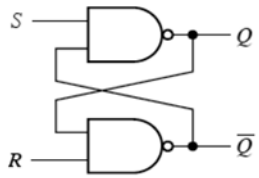


S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

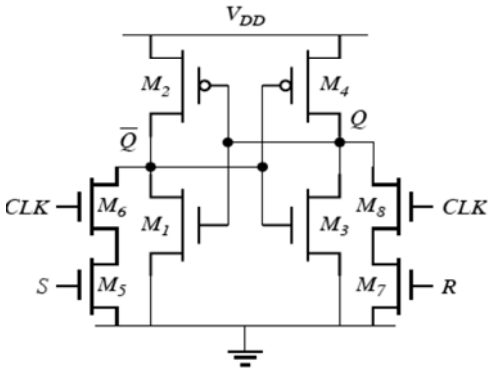
Forbidden State

Cross-Coupled NAND

Cross-coupled NANDs

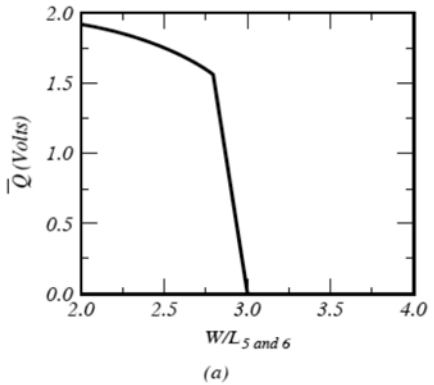


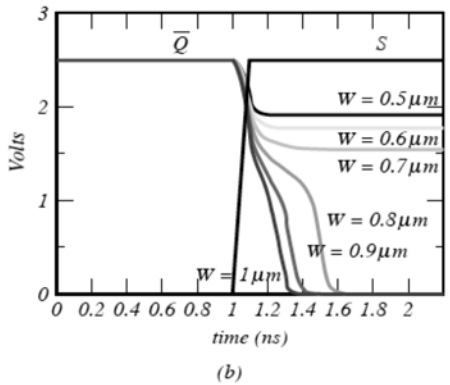
Added clock



This is not used in datapaths any more,
but is a basic building block for memory cell

Sizing Issues



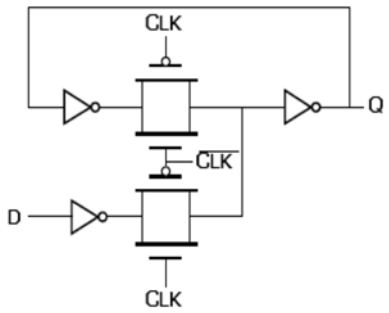


Output voltage dependence on transistor width

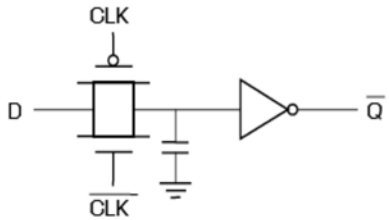
Transient response

Storage Mechanisms

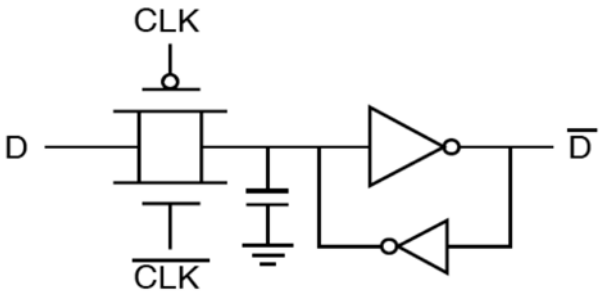
Static



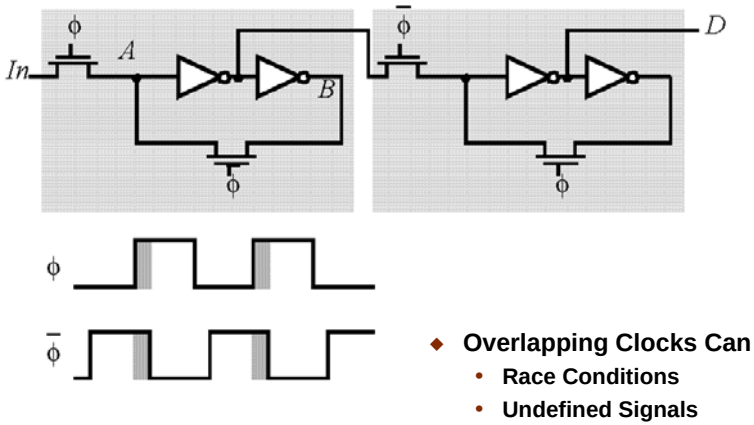
Dynamic (charge-based)



Making a Dynamic Latch Pseudo-Static

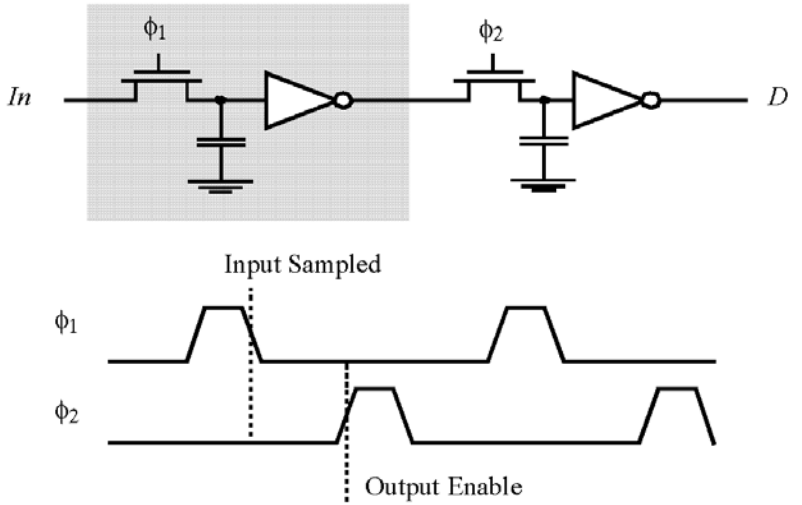


Master-Slave Static Flip-flop

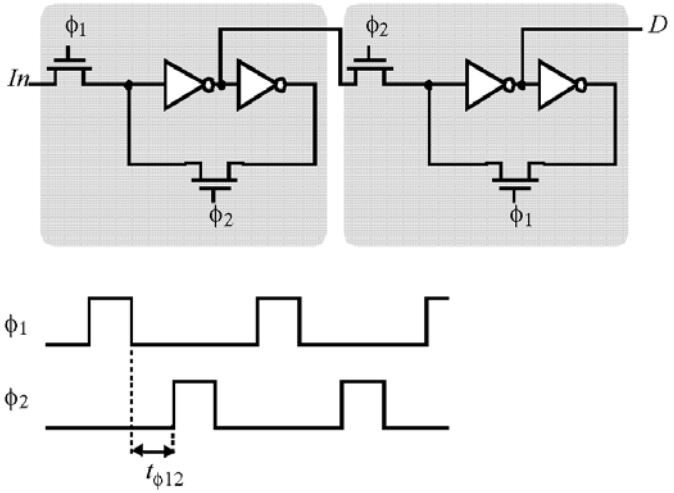


- **Overlapping Clocks Can Cause**
  - **Race Conditions**
  - **Undefined Signals**

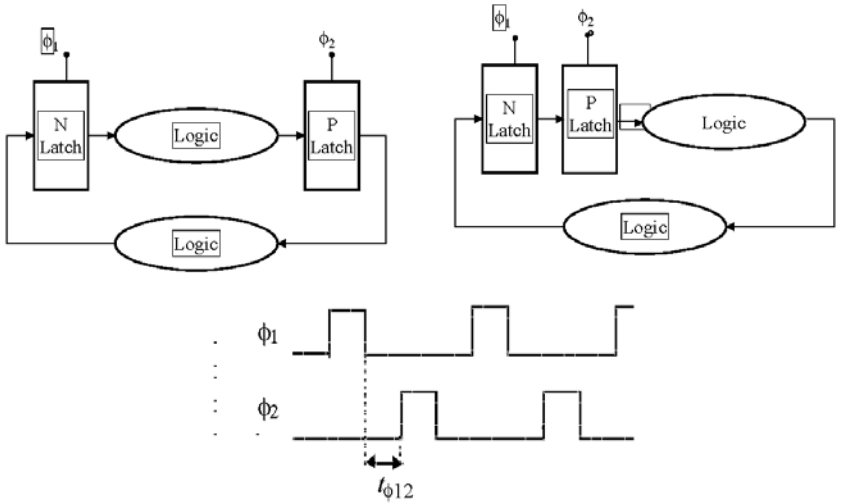
Two-phase dynamic flip-flop



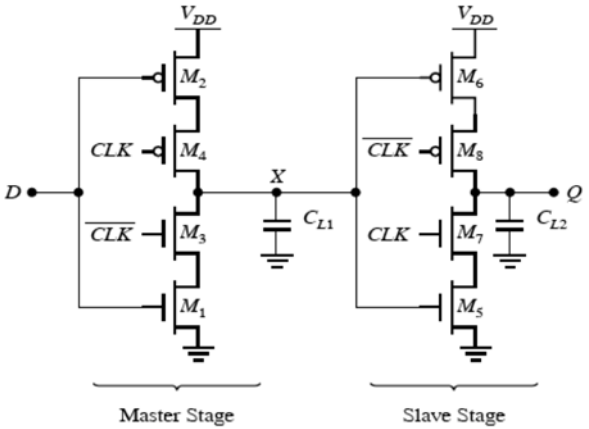
Use 2-phase non-overlapping clocks



Latch + Logic

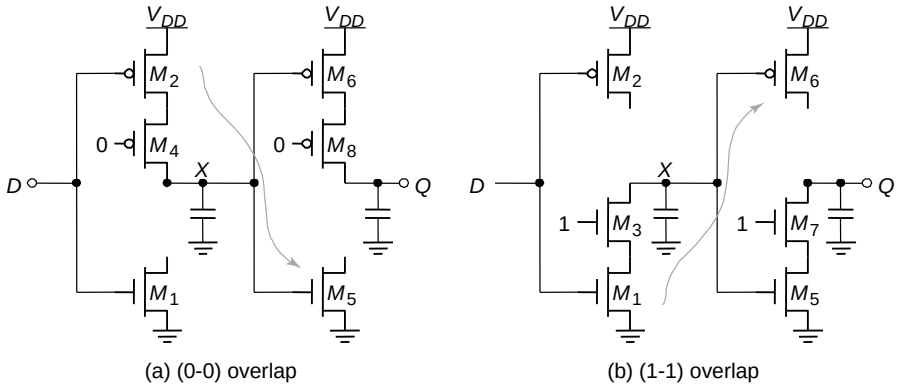


Other Latches/Registers: C²MOS

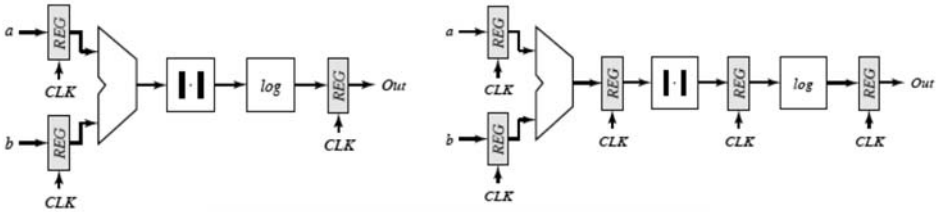


"Keepers" can be added to make circuit pseudo-static

Insensitive to Clock-Overlap



Pipelining

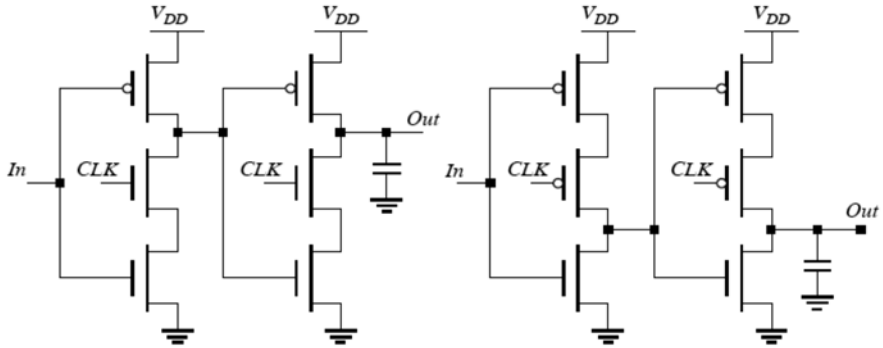


Reference

Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$\lvert a_1 + b_1 \rvert$	
3	$a_3 + b_3$	$\lvert a_2 + b_2 \rvert$	$\log(\lvert a_1 + b_1 \rvert)$
4	$a_4 + b_4$	$\lvert a_3 + b_3 \rvert$	$\log(\lvert a_2 + b_2 \rvert)$
5	$a_5 + b_5$	$\lvert a_4 + b_4 \rvert$	$\log(\lvert a_3 + b_3 \rvert)$

Pipelined

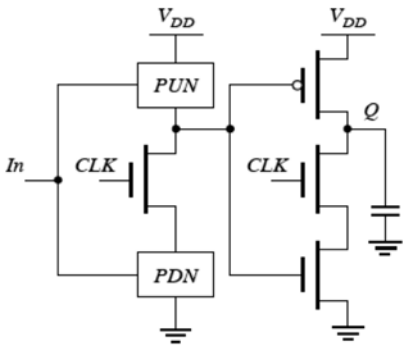
Other Latches/Registers: TSPC



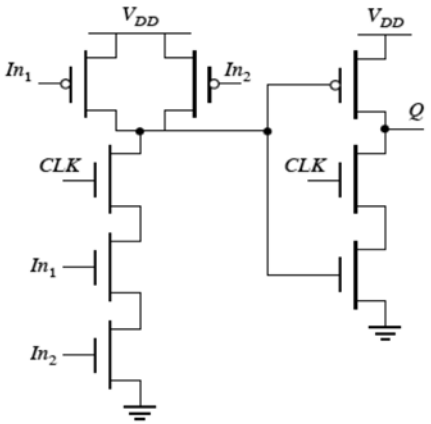
Positive latch
(transparent when CLK= 1)

Negative latch
(transparent when CLK= 0)

Including Logic in TSPC

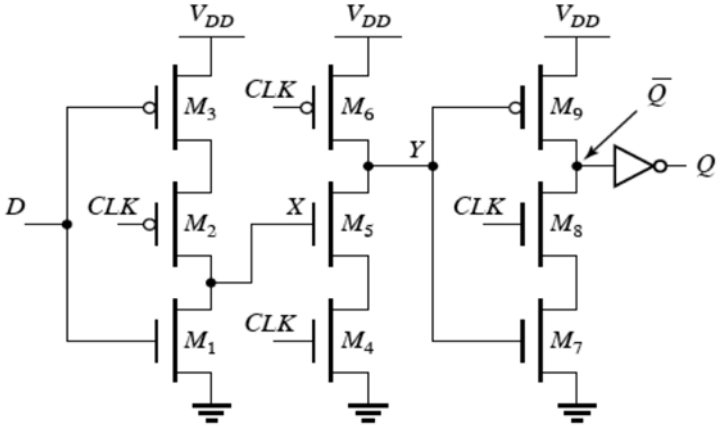


Example: logic inside the latch



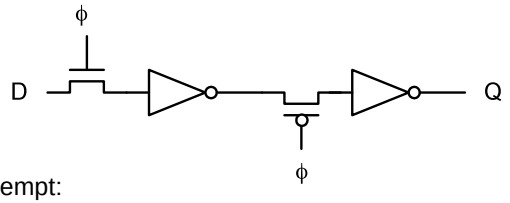
AND latch

TSPC Register

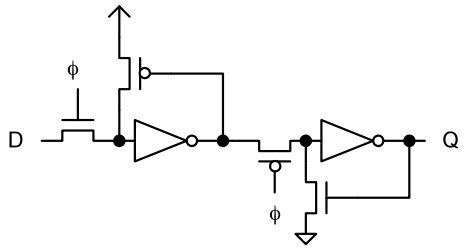


μ–π latches: Poor man's TSPC Latch

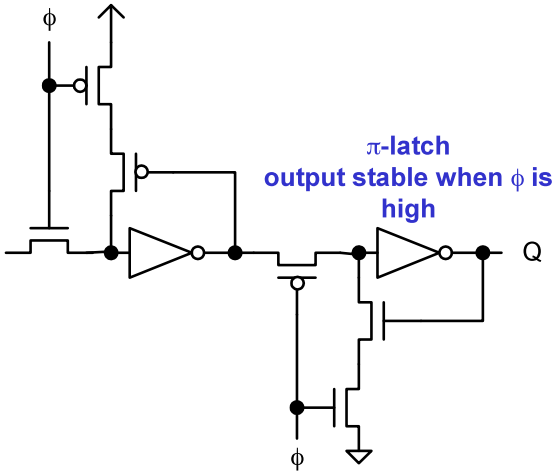
- What is wrong with this TSPC Latch?



- Second attempt:



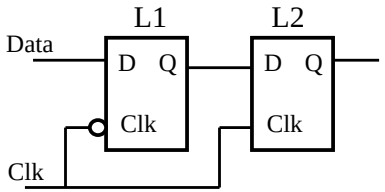
μ–π latches Final solution



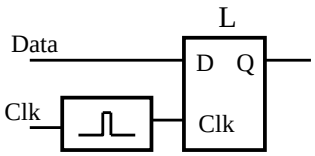
Pulse-Triggered Latches
An Alternative Approach

Ways to design an edge-triggered sequential cell:

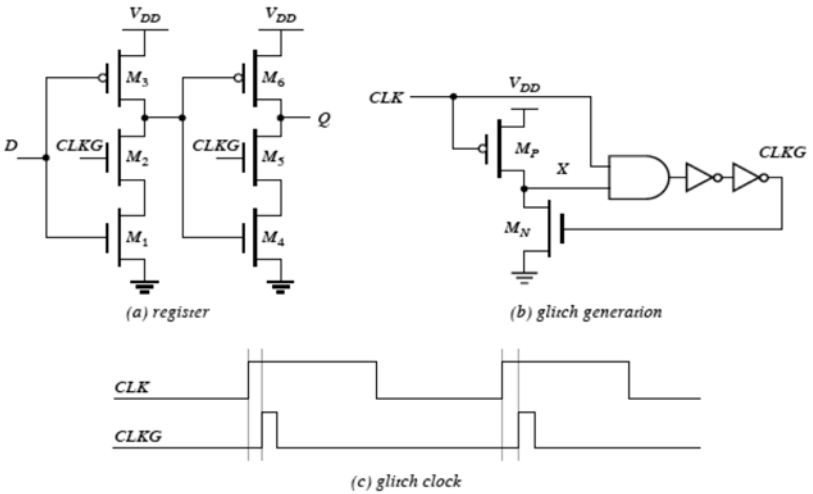
Master-Slave Latches



Pulse-Triggered Latch

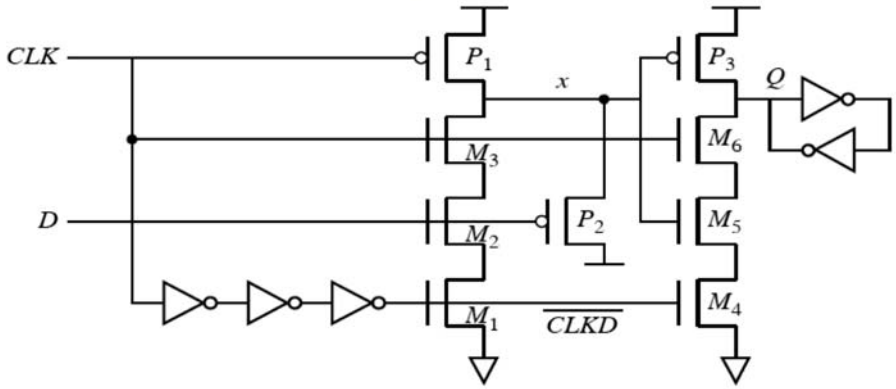


Pulsed Latches

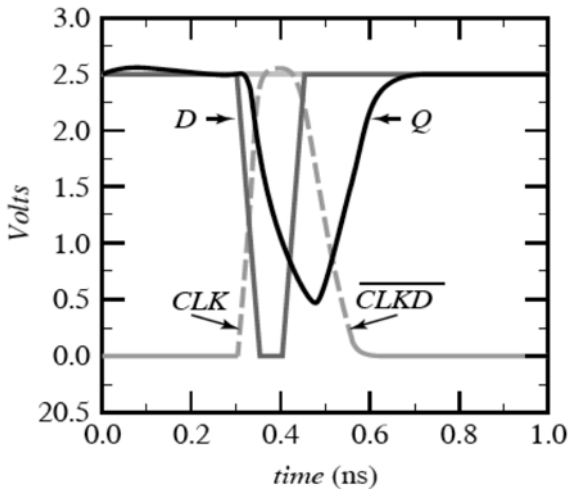


Pulsed Latches

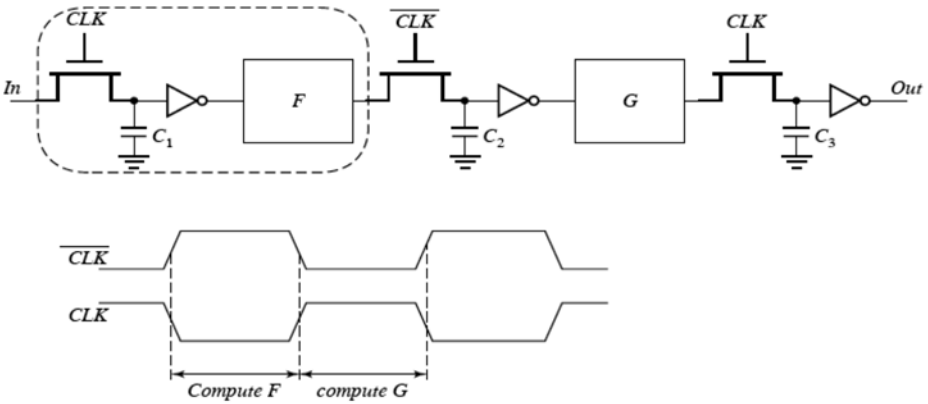
Hybrid Latch – Flip-flop (HLFF), AMD K-6 and K-7 :



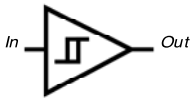
Hybrid Latch-FF Timing



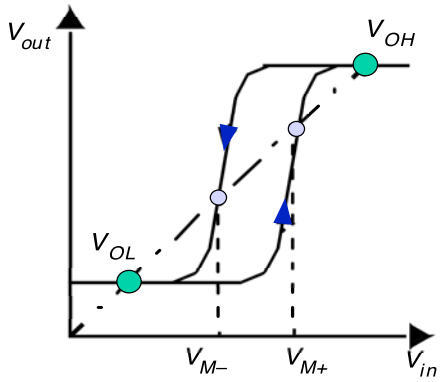
Latch-Based Pipeline



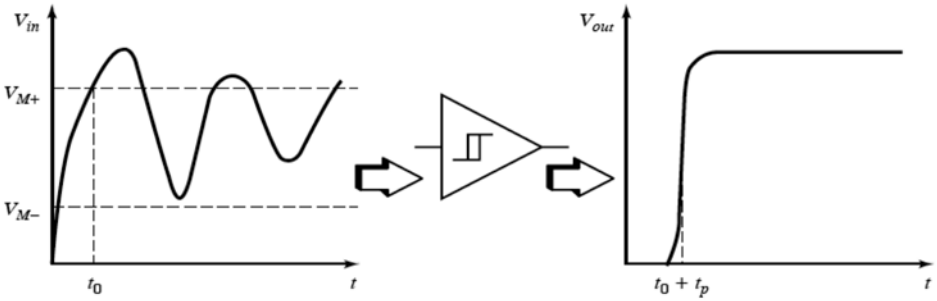
Non-Bistable Sequential Circuits– Schmitt Trigger



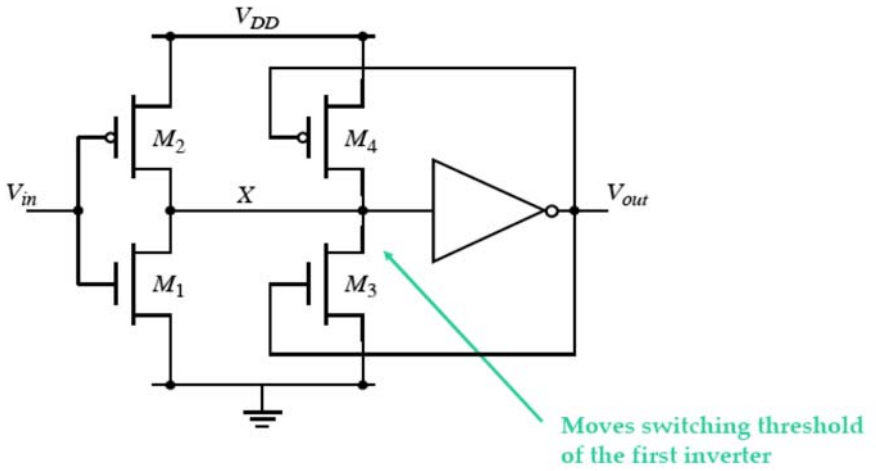
- VTC with hysteresis
- Restores signal slopes



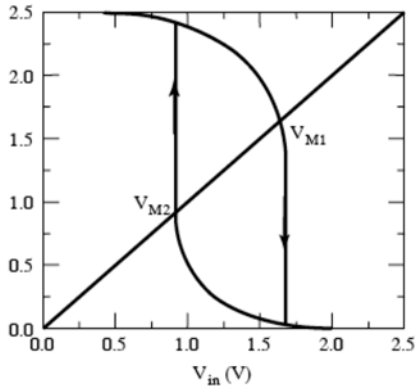
Noise Suppression using Schmitt Trigger



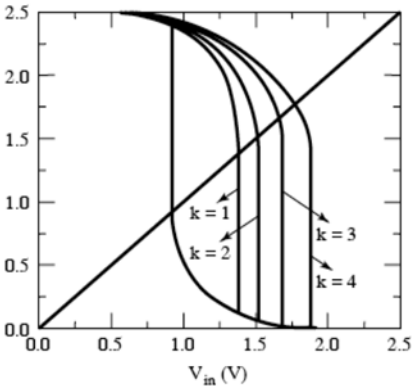
CMOS Schmitt Trigger



Schmitt Trigger Simulated VTC

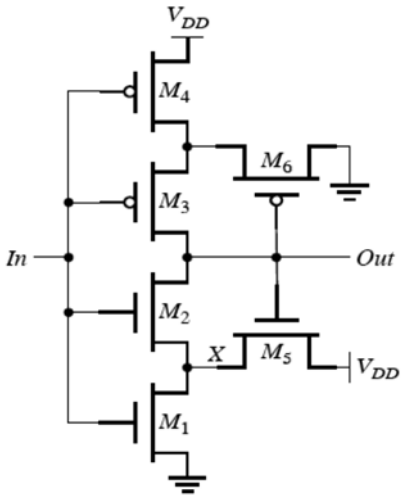


Voltage-transfer characteristics with hysteresis.

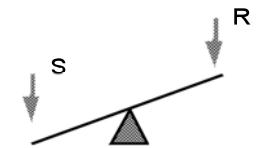


The effect of varying the ratio of the PMOS device M_4. The width is k* 0.5mm.

CMOS Schmitt Trigger (2)



Multivibrator Circuits

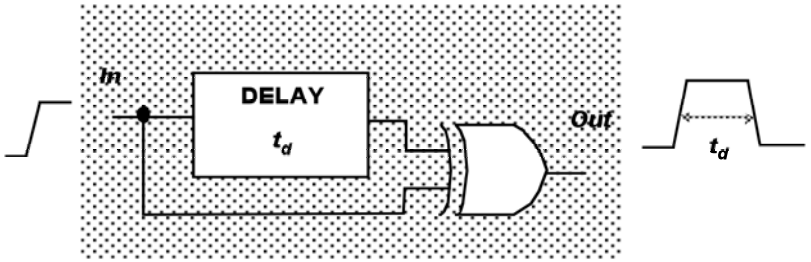


Bistable Multivibrator
flip-flop, Schmitt Trigger

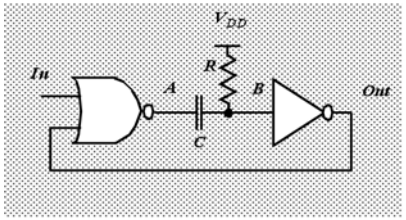
Monostable Multivibrator
one-shot

Astable Multivibrator
oscillator

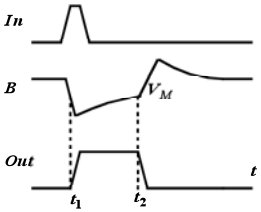
Transition-Triggered Monostable



Monostable Trigger (RC-based)

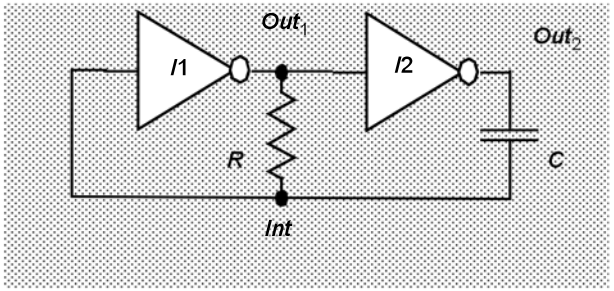


(a) Trigger circuit.



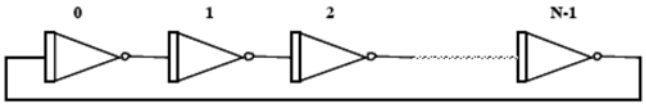
(b) Waveforms.

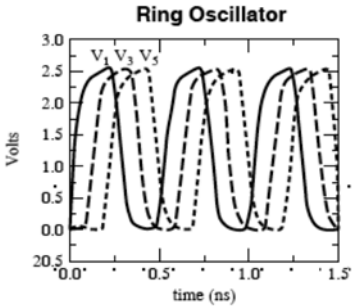
Relaxation Oscillator



$T = 2\ (\log 3)\ RC$

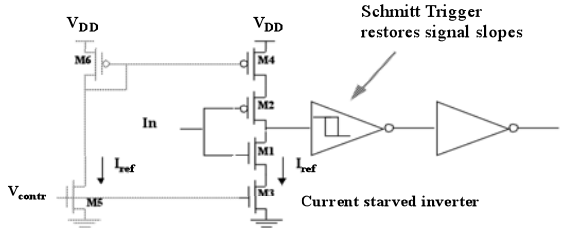
Astable Multivibrators (Oscillators)

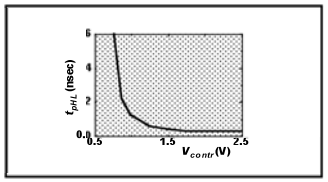




simulated response of 5-stage oscillator

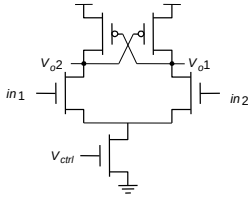
Voltage Controller Oscillator (VCO)



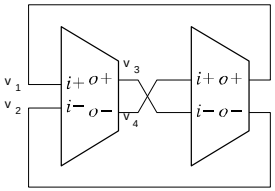


propagation delay as a function of control voltage

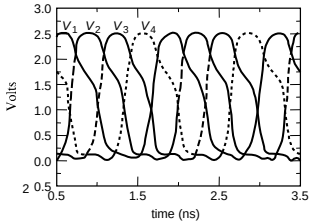
Differential Delay Element and VCO



delay cell



two stage VCO



simulated waveforms of 2-stage VCO